Shin-Etsu

Shin-Etsu Handotai Co.,Ltd.

SOI for High Speed &
Low Power Consumption

SOI Wafer

Solution for High Speed / Low Power Consumption

Mobile
devices

CPU

Communication
Systems

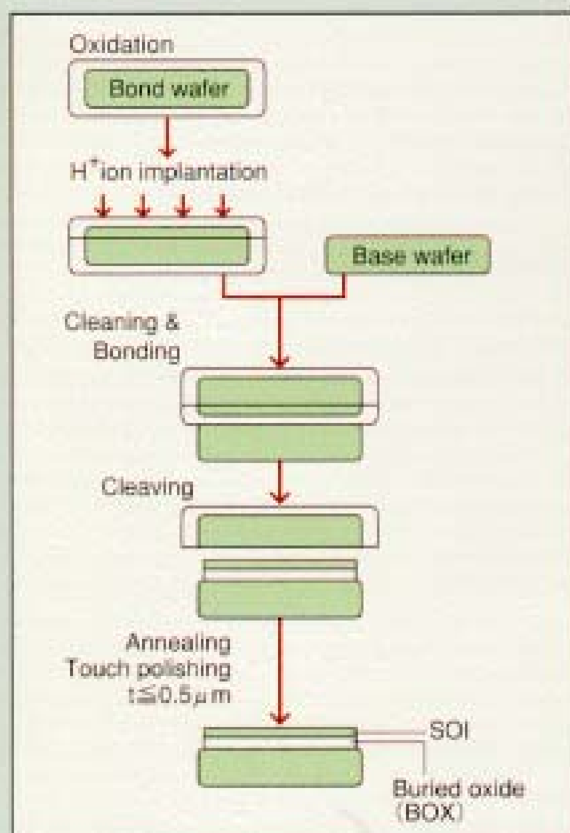
Low Energy

High Speed

Shin-Etsu

UNIBOND® Wafers

Smart-Cut® SOI Process for UNIBOND® Wafers



Specifications

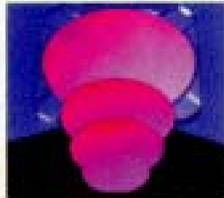
Standard

Diameter		200mm
SOI	thickness	100~200nm
	uniformity	< ±5%
	type	P-type
	resistivity	8.5~11.5Ωcm
	orientation	< 100 >
	Notch/Flat	Notch
BOX	thickness	400nm
	uniformity	< ±2.5%
Base wafer	thickness	725μm
	type	P-type
	resistivity	14~22Ωcm
	orientation	< 100 >
HF defect		< 0.3/cm²
Secco defect		1×E3/cm²
Pipe density		none
Roughness(rms)		<0.2nm
Metal contamination		< 2×E10/cm²
Edge exclusion		5mm

Customized

Diameter		200mm
SOI	thickness	80~1000nm
	uniformity	< ±5%
	type	P-type
	resistivity	Arbitrary
	orientation	< 100 >
BOX	thickness	100~3000nm
	uniformity	< ±2.5%
Base wafer	thickness	725μm
	type	P-type
	resistivity	Arbitrary
	orientation	< 100 >
HF defect, Secco defect		to be specified
Pipe density		none
Roughness(rms)		< 0.2nm
Metal contamination		< 2×E10/cm²
Edge exclusion		5mm

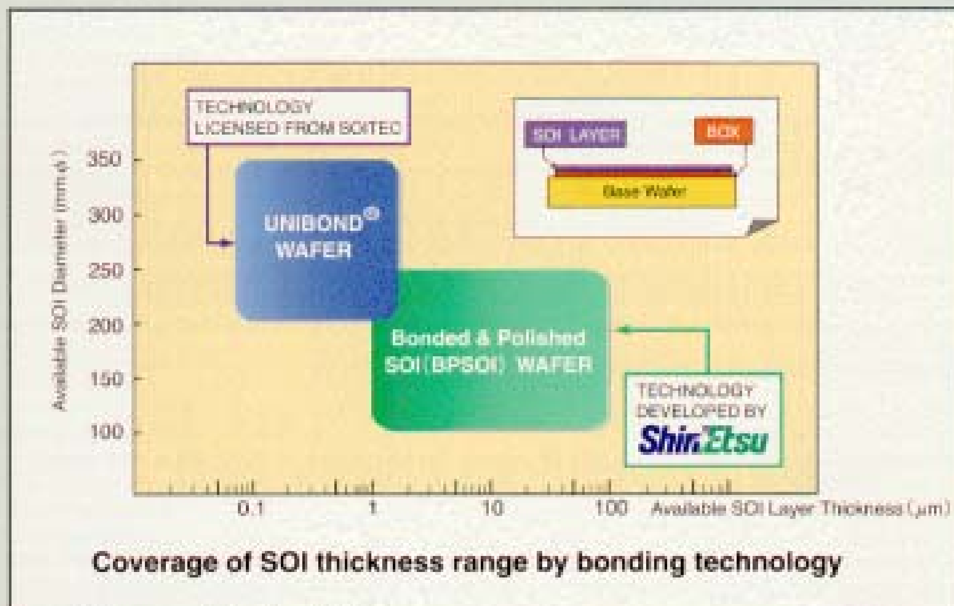
※300mm UNIBOND® wafers are under development.



SOI Wafers are promising material

SOI wafer is total solution material to realize high speed, low power consumption and leak tight due to ideal isolation. It provides flexibility and enhancement for IC designs and development.

SEH Supplies SOI Wafers on Your Requirements



Coverage of SOI thickness range by bonding technology

Smart-Cut® technology is under license from SOITEC

Features of SEH SOI Wafers

1. Excellent thickness uniformity of SOI layer
2. SOI crystal quality equivalent to bulk Si wafer
3. BOX quality equivalent to thermal oxide
4. Low cost and volume supply

Typical Applications

1. High speed / low power / low voltage ICs
2. System-On-Chip
3. High-temperature electronics
4. Radiation-hardened circuits
5. Smart power devices
6. Smart sensors

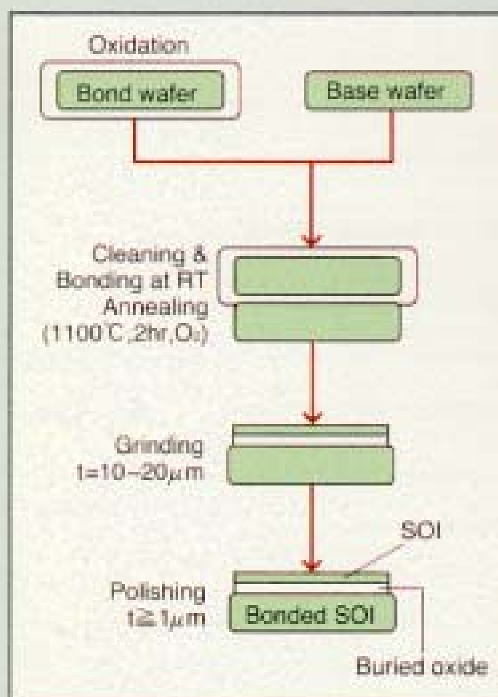
Options

SEH supplies SOI wafers as customers' requirements.

1. SOI layer thickness and resistivity
2. Specification of base and bond wafer
3. Buried oxide layer thickness

Bonded & Polished SOI (BPSOI) Wafers

Process for BPSOI



Specifications

Standard BPSOI Layer

Diameter	100,125,150,200 mm
Crystal orientation	<100><110><111>
Dopant	N Type(P,Sb), P Type(B)
SOI layer thickness	1.0μm or thicker
SOI thickness uniformity	+/-0.5μm (premium for +/-0.3μm)
Buried oxide	0.1μm~4μm
Buried oxide thickness uniformity	+/-5%
Crystal quality	Bulk level
Surface quality	Polished wafer level

Standard Base Wafer

Orientation	<100>
Dopant	N Type (P,Sb), P Type (B)
Resistivity	P (1~30Ωcm) +/-40%, Sb (0.01~0.05Ωcm) +/-30% B (0.01~50Ωcm) +/-30%
Thickness	100mm (525+/-25μm) 125mm (625+/-25μm) 150mm (625+/-25μm or 675+/-25μm) 200mm (725+/-25μm)
Primary flat or notch	100mm (32.5+/-2.5mm) 125mm (42.5+/-2.5mm) 150mm (47.5+/-2.5mm or 57.5+/-2.5mm) 200mm (flat or notch) based on SEMI standard

SOI (Silicon On Insulator) Wafers from SEH

SOI wafers are promising semiconductor material for leading edge devices such as low power and high speed LSIs, smart sensors, and smart power devices.
Shin-Etsu Handotai (**SEH**) has been providing wide thickness range of SOI wafers to meet various customers' requirements by using bonding technology.

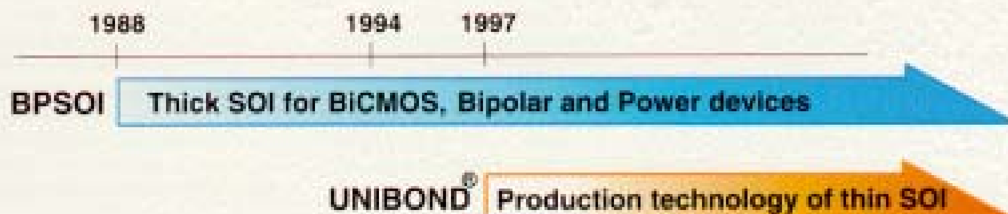
SOI products from SEH

- ☐ **UNIBOND® wafers**
- ☐ **Bonded & Polished SOI (BPSOI) wafers**

History of SOI wafer development in SEH

SEH started development of SOI wafers in 1988. We began with bonded and polished SOI (BPSOI) wafers by precisely controlled grinding and polishing technology, responding to customers' high quality requirements. For thin SOI wafer ($\leq 0.5\mu m$) production, Smart-Cut® technology was introduced in 1997. UNIBOND® wafers are available now for LSI applications.

Technical Development of SOI Wafers in SEH



Precaution

All data presented in this catalog may not be relied upon to represent standard values. Shin-Etsu Handotai reserves the right to change information in this catalog, including product performance standards and specifications, without notice.

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